REMARKS

In an Office Action mailed December 9, 2004, pending claims 1-20 were examined and claim 21 is withdrawn, having been previously canceled in response to a restriction requirement. Claims 1-20 were rejected. In response, Applicants are herein amending claims 1-4, 6-10, 14 and 18, canceling claims 5, 11-13, 15-17 and 19-20, and presenting new claim 22. Applicants respectfully request the reconsideration and allowance of claims 1-4, 6-10, 14, 18 and 22, thereby placing the application in condition for allowance. The total number of independent claims remains no greater than three and the total number of claims remains no greater than twenty. Therefore, no additional fees are owed as a result of the requested claim amendments.

Claims 16 and 17 were rejected under 35 U.S.C. 112, second paragraph, for being indefinite. In response, claims 16 and 17 are canceled to thereby make the rejection moot.

Claims 1-4, 6-8, 11, 14, 16 and 18 were rejected under 35 U.S.C. 102(e) as being anticipated by Tsai et al. (U.S. Pat. Pub. 2003/0080357). In the Tsai et al. integrated circuit of Figure 3A and 3B referenced in the rejection, critical signals such as S1, Clk and D1 are positioned along an edge of an integrated circuit. In the Figure 3 embodiment, the critical signal has no signal shielding between the signal pad and the edge of the integrated circuit. In other words, there is no intervening shielding pad between the edge of the integrated circuit and the critical signal's pad. Also, there is no shielding pad positioned inward toward

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the center of the circuit from a critical signal pad. The Tsai et al. bond pad structure leaves signals susceptible to significant interference and degraded performance. Tsai et al. do not teach or suggest as recited in claim 1 "six shield interconnect pads functioning as shields to the victim interconnect pad, a first and a second of the shield interconnect pads being respectively offset from the second and third sides of a first of the differential pair of victim interconnect pads, a third and a fourth of the shield interconnect pads being respectively offset from the second and third sides of a second of the differential pair of victim interconnect pads, a fifth of the shield interconnect pads being offset from the fourth side of the first of the differential pair of victim interconnect pads, a sixth of the shield interconnect pads being offset from the fourth side of the second of the differential pair of victim interconnect pads, wherein no additional victim interconnect pads are positioned substantially along diagonals of the differential pair of victim interconnect pads". Tsai et al. do not teach or suggest "a shielding group of interconnect pads on a same level of the semiconductor die that electrically shield a predetermined victim interconnect pad also located on the same level of the semiconductor die from noise sources, the victim interconnect pad having first, second, third and fourth sides, the shielding group of shield interconnect pads comprising eight shield interconnect pads, a respective one of the eight shield interconnect pads being respectively offset from each side of the victim interconnect pad, and a respective one of the eight shield interconnect pads being offset diagonally from each corner of the victim interconnect pad, thereby resulting in three of

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the eight shield interconnect pads being aligned along an outer edge of the semiconductor die" as recited in independent claim 14. Tsai et al. do not teach or suggest three rows of interconnect pads and "a plurality of shielding interconnect pads positioned in the first row and in at least one of the second row and the third row, the plurality of shielding interconnect pads positioned radially around a periphery region of the victim interconnect pad and closer to the victim interconnect pad than any of the plurality of interconnects" as recited in new independent claim 22. Applicants therefore request that the rejection under 35 U.S.C. 102(e) on the basis of Tsai et al. be withdrawn.

Claim 5 was rejected under 35 U.S.C. 103(a) as being unpatentable over Tsai et al. in view of O'Connor et al. (U.S. Patent 6,692,272). Claim 5 is herein canceled to make this rejection moot. It should be noted that the combination of Tsai et al. and O'Connor et al. does not teach or suggest the claimed invention of the remaining claims. O'Connor teaches a multi-level bond pad structure for efficient use of signal space along the edge of an integrated circuit die. O'Connor does not teach or suggest correlating victim and shield wire positions in an integrated circuit and does not address the noise interference issues which are overcome in the instant application.

Claims 9-10, 12-13, 17 and 19-20 were rejected under 35 U.S.C. 103(a) as being unpatentable Tsai et al. in view of Lemke et al. (U.S. Patent 6,692,272). Of the remaining claims in this group, each is distinguishable from Tsai et al. as discussed above. Lemke et al. teach an electrical connection with multiple angled and parallel conductors.

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Figure 6 of Lemke et al. was relied upon to form the stated rejection. Lemke et al. does not relate to an integrated circuit or to bond pads. It should be noted that in the Figure 6 connector Lemke et al. uses multiple differential signal conductors, such as S9+ and S9-, are positioned along exposed edges of the connector. The shielding used by Lemke et al., even if argued is taken out of the discrete connector context and applied to integrated circuits, is different from that claimed in the present invention. The conductor positioning taught by Lemke et al. where differential signals are exposed to interference along the edges of a connector does not teach or suggest the recited semiconductor package. Withdrawal of the rejection of the remaining claims on the basis of Tsai et al. in view of Lemke et al. is respectfully requested.

Applicants respectfully request consideration of the amendments and the allowance of claims 1-4, 6-10, 14, 18 and 22, thereby placing the application in condition for allowance. Should issues remain that might be subject to resolution through a telephonic interview, the Examiner is requested to telephone the undersigned at (512) 996-6839.

Respectfully submitted,

By: Robert L. King

Robert L. King
Attorney of Record
Reg. No.: 30,185
Telephone: (512) 996-6839
Fax No.: (512) 996-6854

SEND CORRESPONDENCE TO:

Freescale Semiconductor, Inc.
Customer Number: 23125

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